White Paper

The History of the PCI Bus Architecture

Introduction

It's important to go back in time to the days of the non-intelligent buses such as VESA Local bus, EISA, ISA. These bus structures were in a word, "slow." As CPU speeds increased with Moore's Law, the need for a faster, more intelligent bus emerged. In the early 1990's, Intel invented the Peripheral Component Interconnect (PCI) bus, which had a sweeping effect on the bus structures of the day. The PCI bus began as a 32-bit/ 33 MHz bus capable of 1 Gb/sec of data transfers. But most important was the fact that, unlike its predecessors, it was an intelligent bus. Soon, all servers, workstations and personnel computers were equipped with a PCI bus.

Intel, knowing they had a good thing with the PCI bus, decided to share the technology with the world. This enabled others to build the bridge chips and drove the cost of implementing such a sophisticated bus down dramatically. Now with this low cost, high speed bus, new designs were emerging that solved old dilemmas.

With the PCI bus specification now in the community, one of the dilemmas in the VME world was about to be solved. The VME industry was strapped to a maximum of 21 slots and no way to expand. System designers needed more functionality, especially in the area of I/O. The perfect solution would take the form of a daughter or mezzanine card but not protrude past a single slot mechanical envelope. Such a card would add the needed functionality without expanding the chassis. Now, with inexpensive PCI bridges available, the VME world solved this problem by developing single slot daughter cards we know now as the PCI Mezzanine Card or PMC card. The PMC card combines the electrical characteristics of the PCI bus with the mechanical dimensions of the Common Mezzanine Card or CMC format. The dimensions are similar to one credit card wide and three credit cards long.

VME was the defacto standard for those in need of an industrial, rugged form factor. Despite the adoption of PMCs for additional functionality, the VME lacked a number of features that were quickly becoming very important. Of those, hot swap, more user I/O pins, increased bus bandwidth, and most of all a cost reduction, emerged as the most important criteria for a new design. The solution took the form of a 6U Euro form factor card (just like VME) and was called CompactPCI.

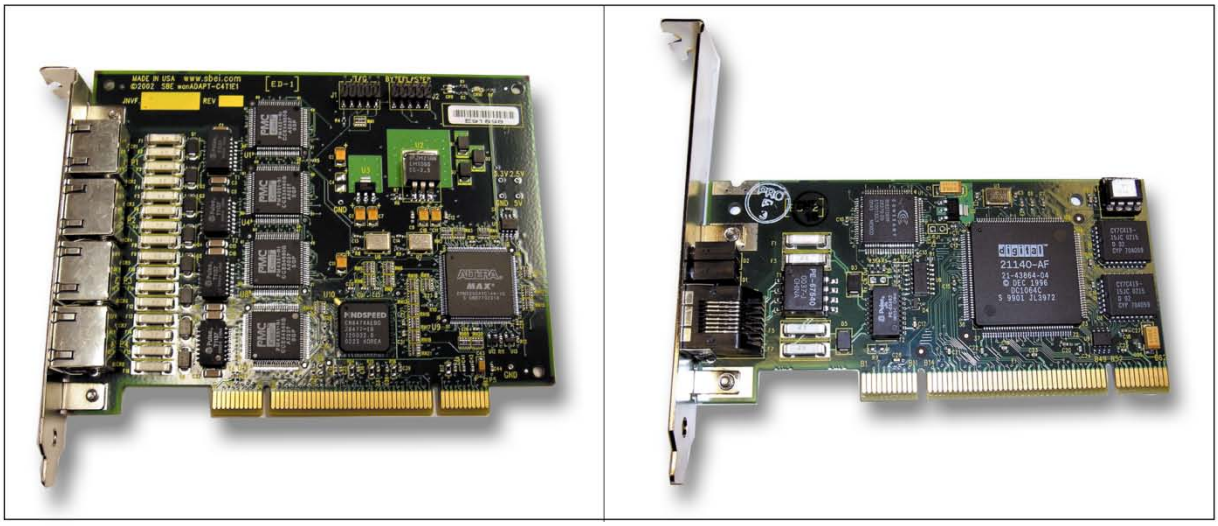
So, with Intel's support, the PCI bus was born and has spawned many new designs and solved many existing challenges. The future is bright with new technology and bus structures as well. The PCI bus continues to increase in speed, a new serial bus coined PCI Express promises data transfer speeds of greater than 80 Gb/s, and the CompactPCI and PMC form factors are expanding with a new form factor called ATCA (Advanced Telecom Computing Architecture) to meet greater power and cooling needs.

The remainder of this paper will concentrate on describing in more detail the PCI bus and subsequent busses derived from it.

PCI Bus

First introduced in the early 1990s, the PCI bus had a sweeping effect on the current bus structures. The PCI bus, with initial data transfer speeds of 1 Gb/sec, was not only much faster than existing buses, but was designed to be more intelligent. Several cards can coexist on the bus simultaneously. Each PCI card contains a set of registers that allows the host processor to identify and properly configure resources at boot up. These registers also facilitate true Plug and Play capability in a PCI environment.

As shown below in the figure, PCI cards can take on several different forms, from short to long and regular to low profile. The bus structures also have several permutations from 32-bit/ 33 MHz to 64-bit/ 66 MHz. Refer to the following table for PCI bus architecture performance capabilities. A standard PCI bus can be up to four slots. Each slot can be any combination listed on the chart below. Electrical signaling is an important part of the PCI specification. The PCI signal is a "reflective" signal meaning that the signal travels to the end of the bus, and as the reflection travels back the other direction, the information is considered valid. The signal voltage levels can be 3.3V, 5V, or Universal. The PCI specification is governed by the PCI-Sig group (http://www.pcisig.com).



Sample PCI Bus Cards

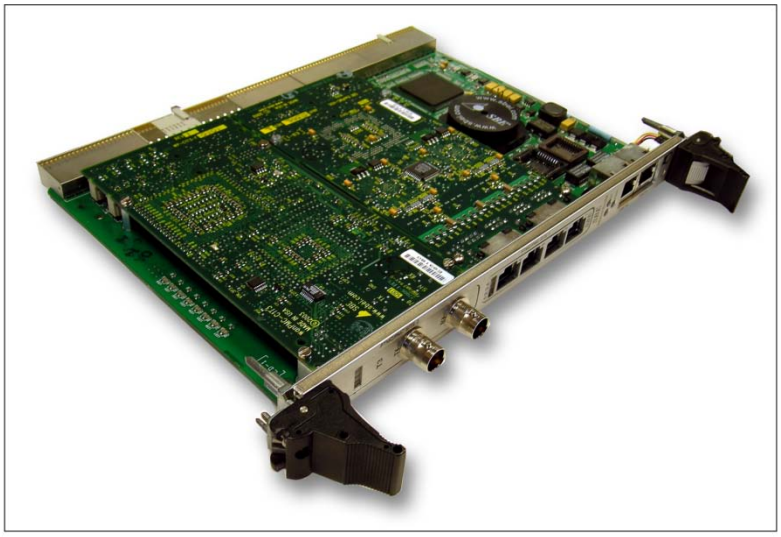
PCI Bus			
Width	**Speed**	**Bandwidth**	
32 bits	33 MHz	132 MB	1 Gb
32 bits	66 MHz	264 MB	2 Gb
64 bits	33 MHz	264 MB	2 Gb
64 bits	66 MHz	512 MB	4 Gb
64 bits	133 MHz*	1024 MB	8 Gb

* Note: PCI-X

The PCI bus has had an incredibly good run and shown great success in the past. However, even at 64-bit/133 MHz, the PCI is running out of gas for some applications. These applications will be much better served by evolving to PCI Express. However, many less demanding interfaces such as T1/E1 and T3/E3 will continue to use the standard PCI bus for years to come.

PMC/PTMC

The PCI Mezzanine Card or PMC evolved from the PCI specification and was developed to solve the need to add more functionality to already overburdened VME systems. An IEEE specification (IEEE1386) governs the electrical and mechanical characteristics of the PMC card. The card measures 3” X 5” and is designed as a mezzanine or daughter card intended to fit between two adjacent boards without extending past a single slot. Along with adding more functionality to a system, PMCs can also serve to make a single base platform more flexible. As an example, the SBE HW400c/M can serve as a TDM switch when equipped with a T1 PMC card. Add a DSP resource card and you immediately have a VOIP Gateway.



Sample PMC card

Where IEEE1386 defines the electrical and mechanical nature of the PMC card, PICMG 2.3 defines the pin out scheme as it pertains to the CompactPCI platform. PICMG 2.3 defines a 32 or 64-bit interface at 33 MHz along with user definable I/O pins available.

Another PICMG specification, PICMG 2.15 was developed to meet the special needs of the Telecom market. This member of the PMC family is referred to as PCI Telecom Mezzanine Card (PTMC) and retains the mechanical as well as the PCI 32-bit electrical specification. Where it differs is in the pin out assignments. The PTMC was designed to allow for at least two planes of data. The PCI is always there at 32 bits and intended as the control plane. In addition, the specification allows for a combination of the following high bandwidth data plane technologies:

- RMII (10/100 Mb Ethernet)
- Gbit Ethernet
- TDM
- Utopia
- POS/PHY

PTMC Interface Configurations

Interface	0	1	2	3	4	5	6	7	>7
Serial Tx/Rx	RESERVED	X	X	X	X	X	X		RESERVED
RMII			X	X					
RMII PHY Management I/F			X	X					
10/100/1000 Ethernet MDI Ports						2	2		
UTOPIA I/II (8-bit)		X		X	X		X		
UTOPIA II (8/16-bit)					X		X		
POS-PHY					X				
Local CT (20 bit)			X	X					
Extended Local CT (32 bit)						X			
USER IO Pins		64	66	6	0	40	4	64	
32-bit PCI	X	X	X	X	X	X	X	X	
64-bit PCI								X	
JTAG	X	X	X	X	X	X	X	X	
SMB	X	X	X	X	X	X	X	X	

Note: In configurations 2 and 3, two of the USER IO pins are located on Jn3, and are identified as USER1Z and USER2Z.

Much like PCI cards, PMC/PTMC cards have had a good success on VME, CompactPCI and custom motherboard platforms. PMC/PTMC cards will be in demand for many years to come.

COMPACTPCI

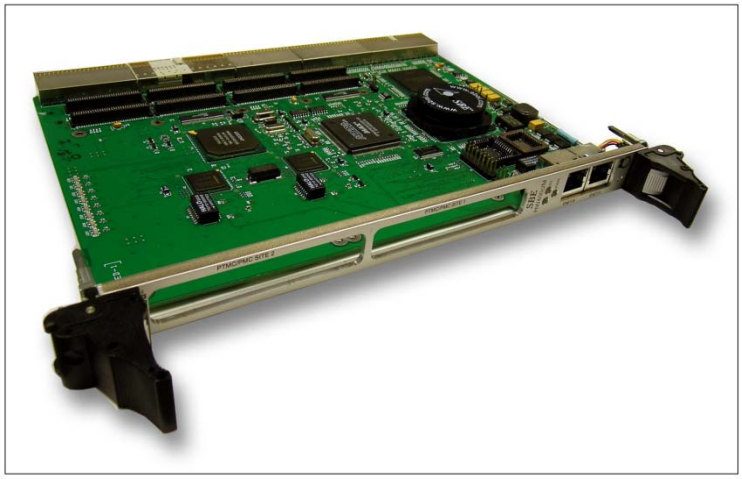
CompactPCI is yet another design spawned from the PCI specification and is also governed by the PICMG organization (www.picmg.com). In the mid 1990's the CompactPCI specification was emerging to meet the needs of those disgruntled with what was perceived to be missing features in VME platforms. Hot swap capability, high-speed bus, more user I/O pins, and lower cost were the most important design criteria. The CompactPCI specification retained the 6U Eurocard form factor with 2 mm pin and socket connectors yielding up to 220 pins. The pins are arranged in groups labeled J1 – J5. J1 and J2 are used exclusively for 32-64 bit/33-66 MHz PCI bus transfers enabling up to 4 Gb of data transfer capability. J3 – J5 are used for user I/O or specifically assigned to another bus structure.

The blade architecture along with pin and socket design makes CompactPCI a very rugged, robust architecture suitable for military, industrial, or telecommunication requirements. CompactPCI boards are inserted from the front of the chassis, and I/O can break out either to the front or through the rear.

Unlike PCI, which only supports up to four cards, the CompactPCI can support eight slots in a chassis. More slots can be enabled with the use of PCI bridging technology. Staged power and ground pins are used to provide true hot swap capability.

The PICMG organization has amassed a plethora of specifications intended to enhance the CompactPCI platform. Without a doubt, the two that standout the most are PICMG 2.5 and 2.16, Computer Telephony Specification and Packet Switching Backplane respectively. The Computer Telephony Specification, more often referred to as H.110, takes the user I/O pins on J4 and assigns them to carry up to 32 lanes of bi-directional TDM data. A CompactPCI board equipped with an H.110 bus can easily be made to function as a TDM switch.

The Packet Switching Backplane, often referred to as 2.16 or PSB, is simply "Ethernet on the backplane". Much like the H.110 above, 2.16 reassigns user I/O pins on J3 to support two sets of 19 full duplex 10/100/1000 Mb/s Ethernet channels. Two CompactPCI cards equipped with PSB could communicate out of band from the PCI bus via Ethernet. The added bonus is due to the fact there are two sets of Ethernet lines, the two boards now have a failover channel. Add an Ethernet switch into the system and now up to 19 boards can communicate in a non-blocking fashion all over Ethernet.



Sample CompactPCI card

The Future: PCI Express, ATCA, AMC…

As CPU speeds and physical access technologies continue to increase, dual 2 GHz servers have become commonplace, and 10 Gb Ethernet is just around the corner. These facts demand that bus structures also keep up. PCI, a parallel style bus structure is essentially exhausted at 64-bit/133 MHz, yielding 8 Gb of bandwidth. With 10 Gb Ethernet on the forefront, however, this clearly won't be enough bandwidth to process the data. To address this emerging "need for speed," Intel has developed a serial bus structure, capable of 80 Gb/sec…that's a 10X increase over traditional PCI. Intel coined this new bus structure PCI Express. To date, there are a small number of servers supporting this new technology, but the future is clear that PCI Express will, like PCI, be deployed in every server on the market.

Embedded form factors are also evolving with the recent PICMG (www.PICMG.com) ratification of the Advanced Telecom Computing Architecture (AdvancedTCA®). This new blade style form factor boasts larger board size to accommodate more components, increased power, and better cooling characteristics. In addition, AdvancedTCA will also adapt to several different high-speed switch fabrics allowing for data bandwidth from 10 Gb to greater than 100 Gb. In the early stage, AdvancedTCA will fully embrace the standard PMC daughter card technology. However, in the future we will see the adoption of yet another form factor, AdvancedTCA Mezzanine Card (AMC). The AMC card will act much like its PMC brother, but will provide more board space and hot swap features.

About NComm

NComm, based in Hampstead, NH, provides turnkey embedded software solutions and hardware platforms that are used by equipment vendors to add Ethernet and WAN interfaces to their products. Developed by NComm's team of engineering and business professionals, our products are designed using the experience obtained by decades of experience in communications software and hardware design and bringing complex products to market.

NComm Trunk Management Software is the Ethernet & WAN de facto standard, embedded by equipment vendors from 3COM to ADC to Sonus Networks and is the most widely used and tested software for Ethernet and WAN OAM. NComm delivers the underpinning, drop-in software technology necessary to build interoperable, standards-compliant WAN access devices including framer configuration, alarming & fault management, PMON, line testing, and signaling. NComm's mission is to reduce their client's time-to-market through turnkey Ethernet, T1, E1, T3, E3, SONET, SDH, APS, Primary Rate ISDN and Sync Status Message telecommunications source code

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